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## DIODE STEP STRESS TESTING PROGRAM

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FINAL REPORT  
FOR  
JANTX 1N5554

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Prepared  
For

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## FOREWORD

This is a summary of the work performed on NASA Contract NAS8-31944. The investigation was conducted for the National Aeronautics and Space Administration, George C. Marshall Space Flight Center, Huntsville, Alabama. The Contracting Officer's Technical Representative was Mr. F. Villella.

The short-term objective of this preliminary study of transistors, diodes, and FETS was to evaluate the reliability of these discrete devices, from different manufacturers, when subjected to power and temperature step stress tests.

The long-term objective is to gain more knowledge of accelerated stress testing for use in future testing of varieties of discrete devices, as well as to determine which type of stress should be applied to a particular type of device or design.



## TABLE OF CONTENTS

	<u>Page</u>
1.0 INTRODUCTION . . . . .	1
2.0 TEST REQUIREMENTS . . . . .	1
2.1 Electrical . . . . .	1
2.2 Stress Circuit . . . . .	1
2.3 Group I - Power Stress . . . . .	2
2.4 Group II - Temperature Stress I . . . . .	2
2.5 Group III - Temperature Stress II . . . . .	2
3.0 DISCUSSIONS OF TEST RESULTS . . . . .	3
3.1 Group I - Power Stress . . . . .	3
3.1.1 Semtech . . . . .	3
3.1.2 Micro Semiconductor . . . . .	3
3.1.3 Statistical Summary - Group I . . . . .	4
3.2 Group II - Temperature Stress I . . . . .	4
3.2.1 Semtech . . . . .	4
3.2.2 Micro Semiconductor . . . . .	5
3.2.3 Statistical Summary - Group II . . . . .	6
3.3 Group III - Temperature Stress II . . . . .	6
3.3.1 Semtech . . . . .	6
3.3.2 Micro Semiconductor . . . . .	6
3.3.3 Statistical Summary - Group III . . . . .	7
4.0 FINAL DATA SUMMARY . . . . .	7
5.0 CONCLUSIONS . . . . .	7
APPENDIX A . . . . .	
APPENDIX B . . . . .	





## LIST OF ILLUSTRATIONS

<u>Figure</u>	<u>Title</u>	<u>Page</u>
1	Power and Temperature Stress Circuit For JANTX1N5554 . . . . .	10
2	Cumulative Percent Failures Versus Junction Temperature, Semtech . . . . .	11
3	Time Steps Versus Junction Temperature, Semtech . . . . .	12
4	Cumulative Percent Failures Versus Junction Temperature, Micro Semiconductor . . . . .	13
5	Time Steps Versus Junction Temperature, Micro Semiconductor . . . . .	14
A-1	S/N 6853, Micro Semiconductor, Magnification 8X.	28
A-2	S/N 6856, Micro Semiconductor, Magnification 8X.	28
A-3	S/N 6824, Semtech, Magnification 11X . . . . .	29
A-4	S/N 6824, Semtech, Magnification 8X . . . . .	29
B-1	S/N 6916, Semtech, Magnification 10X . . . . .	34

## LIST OF TABLES

<u>Table</u>	<u>Title</u>	<u>Page</u>
1	Test Flow Diagram . . . . .	15
2	Parameters and Test . . . . .	16
3	Power Stress Burn-In Conditions . . . . .	16
4	Group I - Power Stress Data Summary . . . . .	18
5	Group II - Temperature Stress I Data Summary .	20
6	Group III - Temperature Stress II Data Summary.	21
7	Final Data Summary . . . . .	22
8	Step Stress Catastrophic Failure Summary . . .	23
9	Step Stress Parametric Failure Summary . . . .	24



## 1.0 INTRODUCTION

DCA Reliability Laboratory, under Contract NAS8-31944 for NASA/Marshall Space Flight Center, has compiled data for the purpose of evaluating the effect of power/temperature step stress when applied to a variety of semiconductor devices. This report covers the switching diode JANTX1N5554 manufactured by SEMTECH and MICRO SEMICONDUCTOR.

A total of 48 samples from each manufacturer were submitted to the process outlined in Table 1. In addition, two control sample units were maintained for verification of the electrical parametric testing.

## 2.0 TEST REQUIREMENTS

### 2.1 Electrical

All test samples were subjected to the electrical tests outlined in Table 2 after completing the prior power/temperature step stress point. These tests were performed using the Fairchild Model 600 high-speed computer-controlled tester. Additional bench testing was also required on the devices.

### 2.2 Stress Circuit

The test circuit shown in Figure 1 was used to power all of the test devices during the power/temperature stress conditions. The voltage was set by  $V_F$  and the current was varied in order to comply with the specified power rating for this device. At least one of the devices was subjected to maximum rated power (MRP). All remaining devices were subjected to no less than 90% of MRP. See Figure 1 for load resistance values and voltages.



### 2.3 Group I - Power Stress

Thirty-two units, 16 from each manufacturer, were submitted to the Power Stress Process. The diodes were stressed in 500-hour steps at 50, 100, 125, 150 and 175 percent of maximum rated power for 2500 hours or until 50% or more of the devices in a sample lot failed.\* Electrical measurements were performed on all specified electrical parameters after each power step. See Table 1.

### 2.4 Group II - Temperature Stress I

Thirty-two units, 16 from each manufacturer, were submitted to the Temperature Stress, I Process. Group II was subjected to 1600 hours of stress at maximum rated power in increments of 160 hours. The temperature was increased in steps of 25°C, commencing at 75°C and terminating at 300°C or until 50% or more of the devices failed.\* Electrical measurements were performed on all specified electrical parameters after each temperature step. See Table 1.

### 2.5 Group III - Temperature Stress II

Thirty-two units, 16 from each manufacturer, were submitted to the Temperature Stress II Process. Group III was subjected to 112 hours of stress at maximum rated power in increments of 16 hours. The temperature was increased in steps of 25°C, commencing at 150°C and terminating at 300°C or until 50% or more of the devices in a sample lot failed.\* Electrical measurements were performed on all specified electrical parameters after each temperature step. See Table 1.

\* Conditions for failure:

- A) Open or short
- B) Leakage exceeds the maximum limit by 100 times
- C) Other parameters exceed MIL limits by 50% or more.





### 3.0 DISCUSSION OF TEST RESULTS

#### 3.1 Group I - Power Stress

3.1.1 Semtech. The Semtech sample lot completed the entire 2500-hour Group I Testing with six catastrophic failures. The first failure occurred 500 hours into the 100% MRP step. Serial number 6825 failed the maximum  $I_R$  limit. The next failure occurred 500 hours into the 125% MRP step. Serial number 6821 failed the maximum  $I_R$  limit. Serial number 6827 was removed from the Group I Testing 50 hours into the 150% MRP step as a visual reject due to handling. The next catastrophic failure occurred 150 hours into the 150% MRP step. Serial number 6906 failed the maximum  $I_R$  limit. The last three failures occurred 250 hours into the 150% MRP step. Serial number 6824 was removed from the Group I Testing as a visual catastrophic failure.\* Serial numbers 6902 and 6905 failed the maximum  $I_R$  and minimum  $V_{F1}$ ,  $V_{F2}$  limits. Typical characteristics of this sample lot's performance were:

- 1) The mean value for  $I_R$  changed 2.76 $\mu$ A from an initial mean of 163.5nA to a final mean of 2.92 $\mu$ A.
- 2) The mean value for  $V_F$ , changed 0.037V from an initial mean of 1.106V to a final mean of 1.143V.
- 3) The mean value for  $V_{F2}$  changed 75.9mV from an initial mean of 821.9mV to a final mean of 897.8mV.

The control units for this sample lot remained constant throughout the entire Group I Testing.

3.1.2 Micro Semiconductor. The Micro Semiconductor sample lot completed 2250 hours of Group I Testing before the

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\* See Table 8 for explanation.



lot was stopped because 50% of the devices failed. The first two failures occurred 10 hours into the 175% MRP step. Serial numbers 6852 and 6859 were removed from the Group I Testing as visual catastrophic failures.\* The next failure occurred 25 hours into the 175% MRP step. Serial number 6853 failed the maximum  $I_R$  limit. The next three failures occurred 150 hours into the 175% MRP step. Serial numbers 6851, 6858, and 6860 were removed from the Group I Testing as visual catastrophic failures.\* The last two failures occurred 250 hours into the 175% MRP step. Serial number 6854 failed the maximum  $I_R$  limit. Serial number 6856 was removed from the Group I Testing as a visual catastrophic failure.\* Typical characteristics of this sample lot's performance were:

- 1) The mean value for  $I_R$  changed  $1.82\mu A$  from an initial mean of  $51.90nA$  to a final mean of  $1.87\mu A$ .
- 2) The mean value for  $V_{F1}$  changed  $0.024V$  from an initial mean of  $1.033V$  to a final mean of  $1.057V$ .
- 3) The mean value for  $V_{F2}$  changed  $5.3mV$  from an initial mean of  $841.1mV$  to a final mean of  $846.4mV$ .

The control units for this sample lot remained constant throughout the entire Group I Testing.

3.1.3 Statistical Summary - Group I. Table 4 outlines the results of Group I - Power Stress Process for each of the electrical parameters and all measurement points for both Semtech and Micro Semiconductor.

3.2 Group II - Temperature Stress I

3.2.1 Semtech. The Semtech sample lot completed 1440 hours of Group II Testing before the lot was stopped because

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\* See Table 8 for explanation.



more than 50% of the devices failed. The first failure occurred 160 hours into the 175°C-temperature step. Serial number 6834 failed the maximum  $I_R$  limit. The next four failures occurred 160 hours into the 200°C-temperature step. Serial numbers 6830, 6910, 6913, and 6914 failed the maximum  $I_R$  limit. The last four failures occurred 160 hours into the 275°C-temperature step. Serial numbers 6828, 6833, 6909 and 6916 failed the maximum  $I_R$  limit. Typical characteristics of this sample lot's performance were:

- 1) The mean value for  $I_R$  changed 451.21 $\mu$ A from an initial mean of 187.8nA to a final mean of 451.40 $\mu$ A.
- 2) The mean value for  $V_{F1}$  changed .004V from an initial mean of 1.121V to a final mean of 1.117V.
- 3) The mean value for  $V_{F2}$  changed 7.9mV from an initial mean of 896.3mV to a final mean of 888.4mV.

The control units for this sample lot remained constant throughout the entire Group II Testing.

3.2.2 Micro Semiconductor. The Micro Semiconductor sample lot completed the entire 1600-hour Group II Testing with two catastrophic failures. The two failures occurred 160 hours into the 300°C-temperature step. Serial numbers 6868 and 6877 failed the maximum  $I_R$  limit. Typical characteristics of this sample lot's performance were:

- 1) The mean value for  $I_R$  changed 144.96 $\mu$ A from an initial mean of 41.41nA to a final mean of 145.00 $\mu$ A.
- 2) The mean value for  $V_{F1}$  changed .025V from an initial mean of 1.051V to a final mean of 1.076V.
- 3) The mean value for  $V_{F2}$  changed 9.2mV from an initial mean of 890.1mV to a final mean of 899.3mV.



The control units for this sample lot remained constant throughout the entire Group II Testing.

3.2.3 Statistical Summary - Group II. Table 5 outlines the results of Group II - Temperature Stress I Testing for each of the three electrical parameters and all measurement points for both Semtech and Micro Semiconductor.

3.3 Group III - Temperature Stress II

3.3.1 Semtech. The Semtech sample lot completed 48 hours of Group III Testing before the lot was stopped with one catastrophic and eight parametric failures. The catastrophic failure occurred 16 hours into the 200°C-temperature step. Serial number 6840 failed the maximum  $I_R$  limit. Typical characteristics of this lot's performance were:

- 1) The mean value for  $I_R$  changed 15.41 $\mu$ A from an initial mean of 202.0nA to a final mean of 15.61 $\mu$ A.
- 2) The mean value for  $V_{F1}$  changed .030V from an initial mean of 1.119V to a final mean of 1.149V.
- 3) The mean value for  $V_{F2}$  changed 16.3mV from an initial mean of 881.6mV to a final mean of 897.90mV.

The control units for this sample lot remained constant throughout the entire Group III Testing.

3.3.2 Micro Semiconductor. The Micro Semiconductor sample lot completed the entire 112 hours of Group III Testing with no catastrophic failures. Typical characteristics of this lot's behavior were:

- 1) The mean value for  $I_R$  changed 4.68 $\mu$ A from an initial mean of 73.13nA to a final mean of 4.75 $\mu$ A.
- 2) The mean value for  $V_{F1}$  changed .013V from an initial mean of 1.044V to a final mean of 1.057V.





- 3) The mean value for  $V_{F2}$  changed 1.8mV from an initial mean of 886.0mV to a final mean of 887.8mV.

The control units for this sample lot remained constant throughout the entire Group III Testing.

3.3.3 Statistical Summary - Group III. Table 6 outlines the results of Group III - Temperature Stress II Testing for each of the three electrical parameters and all measurement points for both Semtech and Micro Semiconductor.

#### 4.0 FINAL DATA SUMMARY

Table 7 statistically summarizes the change in the mean value from the zero-hour data to the final data. The graphs of Figures 2 and 4 plot the cumulative percent failures versus the temperature stress level for Group II - Temperature Stress I, and Group III - Temperature Stress II. The graphs of Figures 3 and 5 plot the time step for Group II (160 hours) and Group III (16 hours) versus the temperature  $T_1$  and  $T_2$  calculated from Figures 2 and 4. Tables 8 and 9 summarize the failures encountered for all three stress groups. The failures are separated into two categories: catastrophic failures in Table 8 and parametric failures in Table 9. The data from Table 8 was used as a source for the graphs in Figures 2 and 4. Figures 2 and 4 were used as a source for the graphs in Fig. 3 & 5 respectively. Junction temperature is plotted on an inverse hyperbolic scale.

#### 5.0 CONCLUSIONS

An overall view of the test results indicate that the Micro Semiconductor diodes are more durable than the





Semtech diodes. In both Group II and III Tests, the MSC lots had fewer failures which also occurred later in the testing than the Semtech lot. In the Group I Testing the MSC lot was stopped 250 hours before the end of the process but all eight failures occurred in the 175% MRP step. The six Semtech failures occurred in lower MRP steps.

Failure analysis was performed on Group I and Group II because of an apparent failure mode throughout the testing. Almost all of the Semtech failures and many of the MSC failures were due to excessive  $I_R$  leakage. In addition, the remaining MSC devices which failed were still within the electrical limits of the test when they became visual failures due to loss of their anode leads. This suggests these structural failures were caused by exceeding the thermal design limits of the parts.

In the case of the Semtech parts, the curve trace at peak inverse voltage (PIV) indicates a condition of surface instability due to contamination. This contamination can move under the influence of temperature and bias. The analyzed sample are  $I_R$  rejects because their breakdowns have drifted below 1000 volts. The hard, stable breakdown of these sample indicates that there is no junction damage. The most probable cause of the lowered breakdown voltage is a change in the concentration of surface impurities on the P-N junction.

When there is a slight concentration of impurities of the same polarity as the high resistivity side of the junction (not sufficient to cause inversion) then that resistivity will be raised. This in turn will raise the breakdown voltage. Upon migration of these protective charges away from the vicinity of the junction,



the resistivity and the breakdown will fall. The hard breakdown curves of these samples taken together with their acceptable leakage levels at 1000 volts bias during earlier tests, suggests that the surface charge migration mechanism as described above was the cause of the failures.

A plot showing the Cumulative Failure distribution for Groups II and III Testing was drawn for the Semtech sample lot (Figures 2 and 3), but a complete graph could not be drawn for the Micro Semiconductor sample lot because of an insufficient number of failure points in the Group II Testing and an absence of failure points in the Group III Testing. Figures 2 and 3 display the Semtech sample lot used to calculate an activation energy of 2.42eV.

A broken circle around a marked point on the graph indicates a freak failure not calculated as as part of the regression line. A solid circle around a marked point indicates an isolated failure point. The regression line was calculated using the least squares method.

The activation energy was calculated from the formula:

$$E = \left[ \ln \left( \frac{t_1}{t_2} \right) \right] \left[ \frac{8.63 \times 10^{-5} \text{ eV/}^\circ\text{K}}{\left( \frac{1}{T_1 + 273} \right) - \left( \frac{1}{T_2 + 273} \right)} \right] \text{ eV}$$

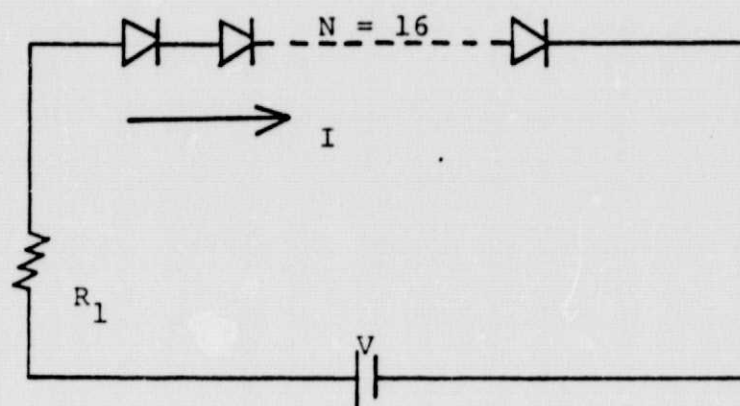
Where:

- $t_1$  = step of Group II - Temp Stress I = 160 hrs.
- $t_2$  = step of Group III - Temp Stress II = 16 hrs.
- $T_1$  = temperature in  $^\circ\text{C}$  of 16% failure for Group II.
- $T_2$  = temperature in  $^\circ\text{C}$  of 16% failure for Group III.



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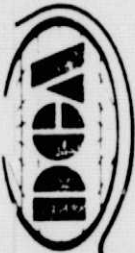
SWITCHING DIODES



$$R_1 = 1V/I \pm 1\%$$

$$P_d = IE$$

FIGURE 1  
Power and Temperature Stress Circuit



SEMTECH

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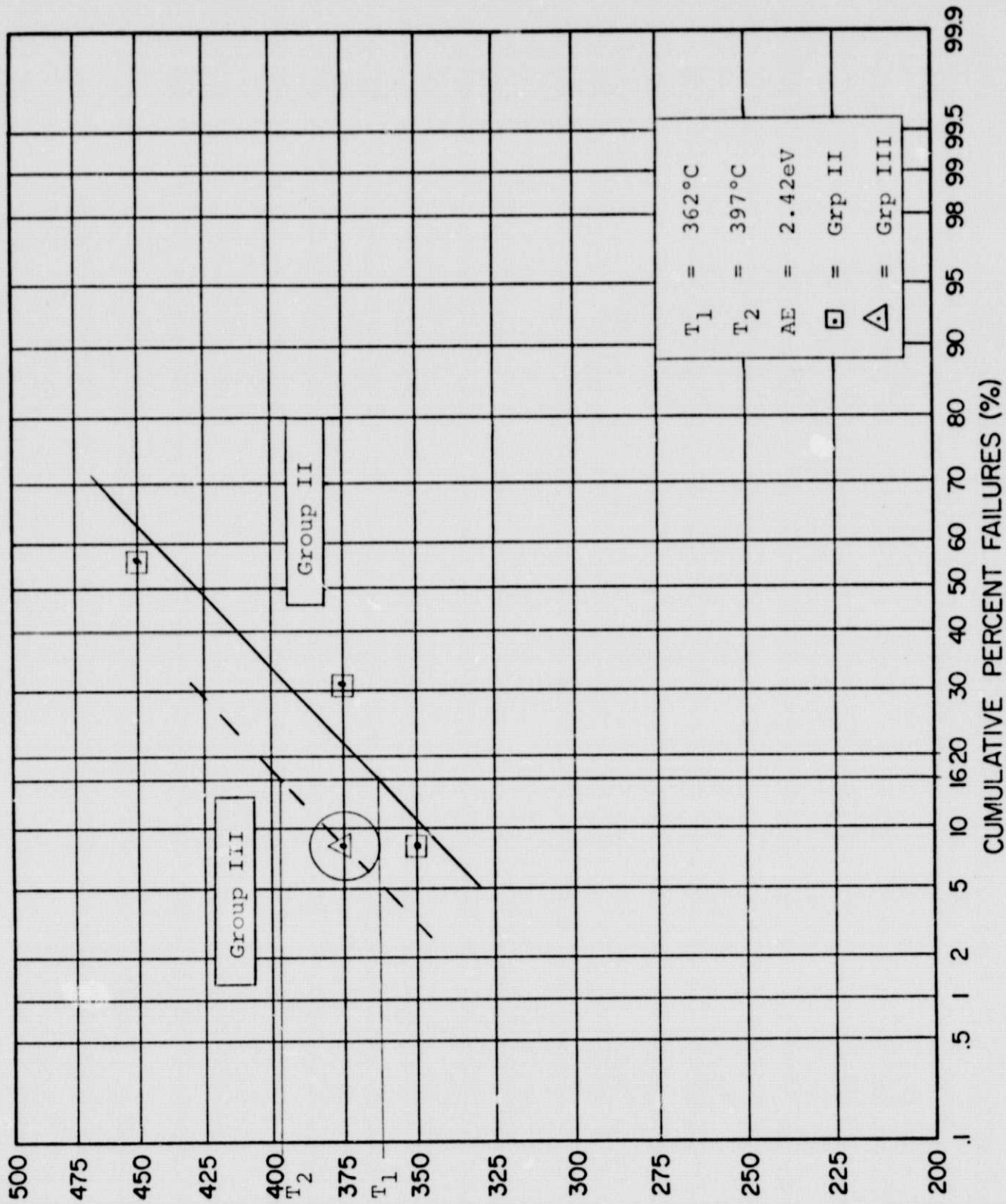


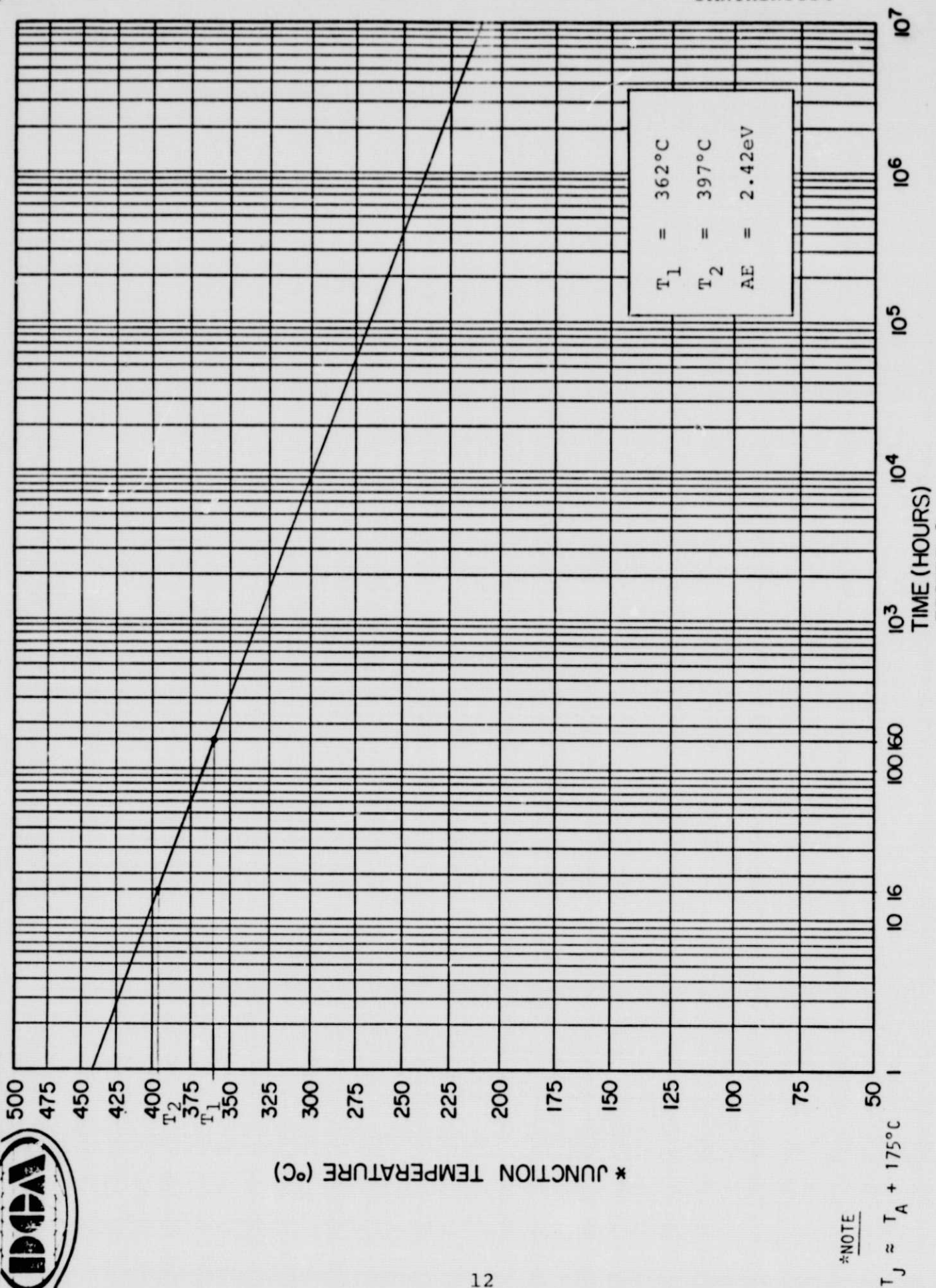
FIGURE 2

Cumulative Percent Failures Versus Junction Temperature, Semtech

\*NOTE

$T_J \approx T_A + 175^{\circ}\text{C}$





Time Steps Versus Junction Temperature, Semtech

FIGURE 3

\*NOTE

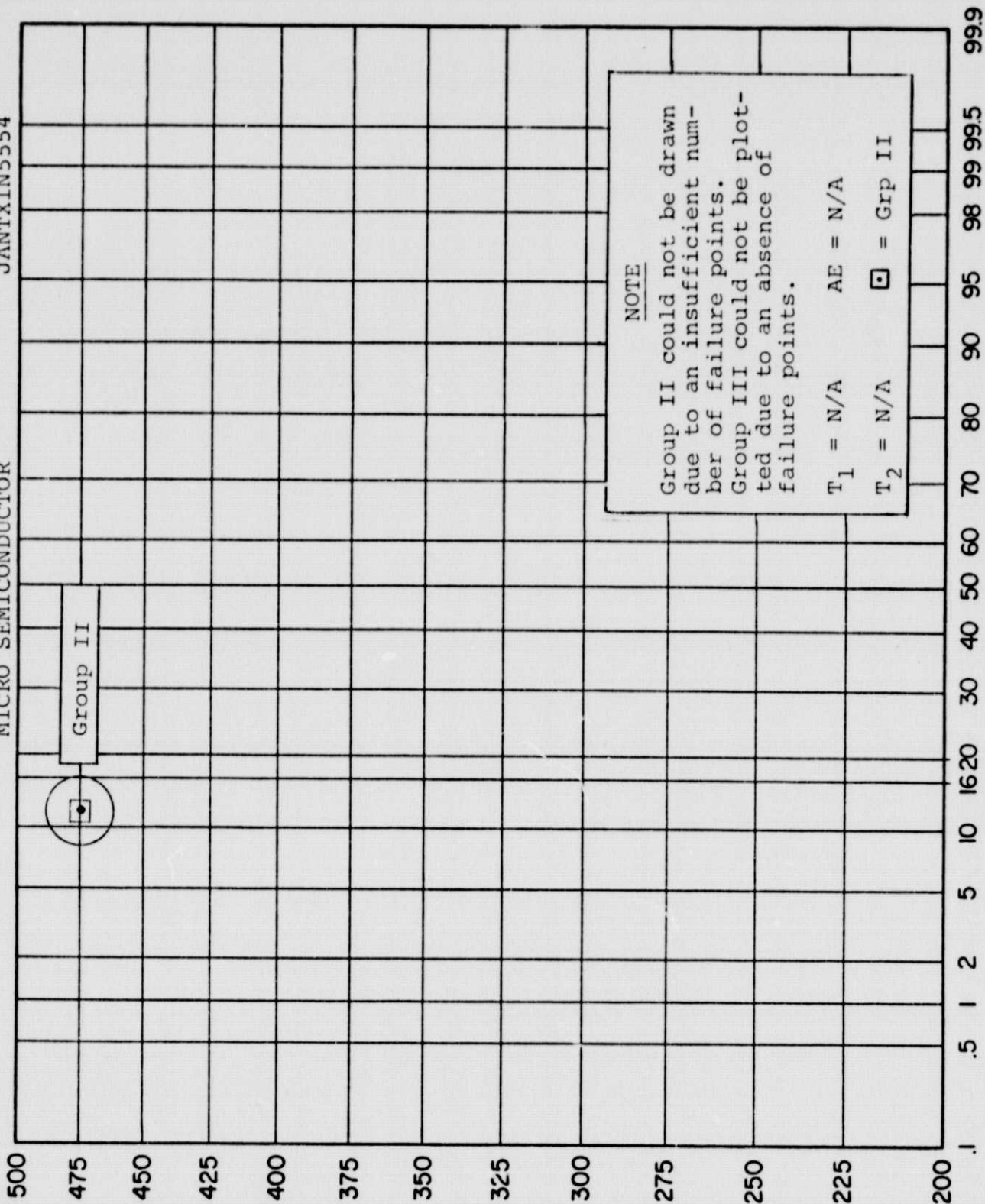
$$T_J \approx T_A + 175^\circ\text{C}$$



MICRO SEMICONDUCTOR

JANTX1N5554

JANTX1N5554



\* JUNCTION TEMPERATURE (°C)

\*NOTE

$T_J \approx T_A + 175^\circ\text{C}$

CUMULATIVE PERCENT FAILURES (%)

FIGURE 4

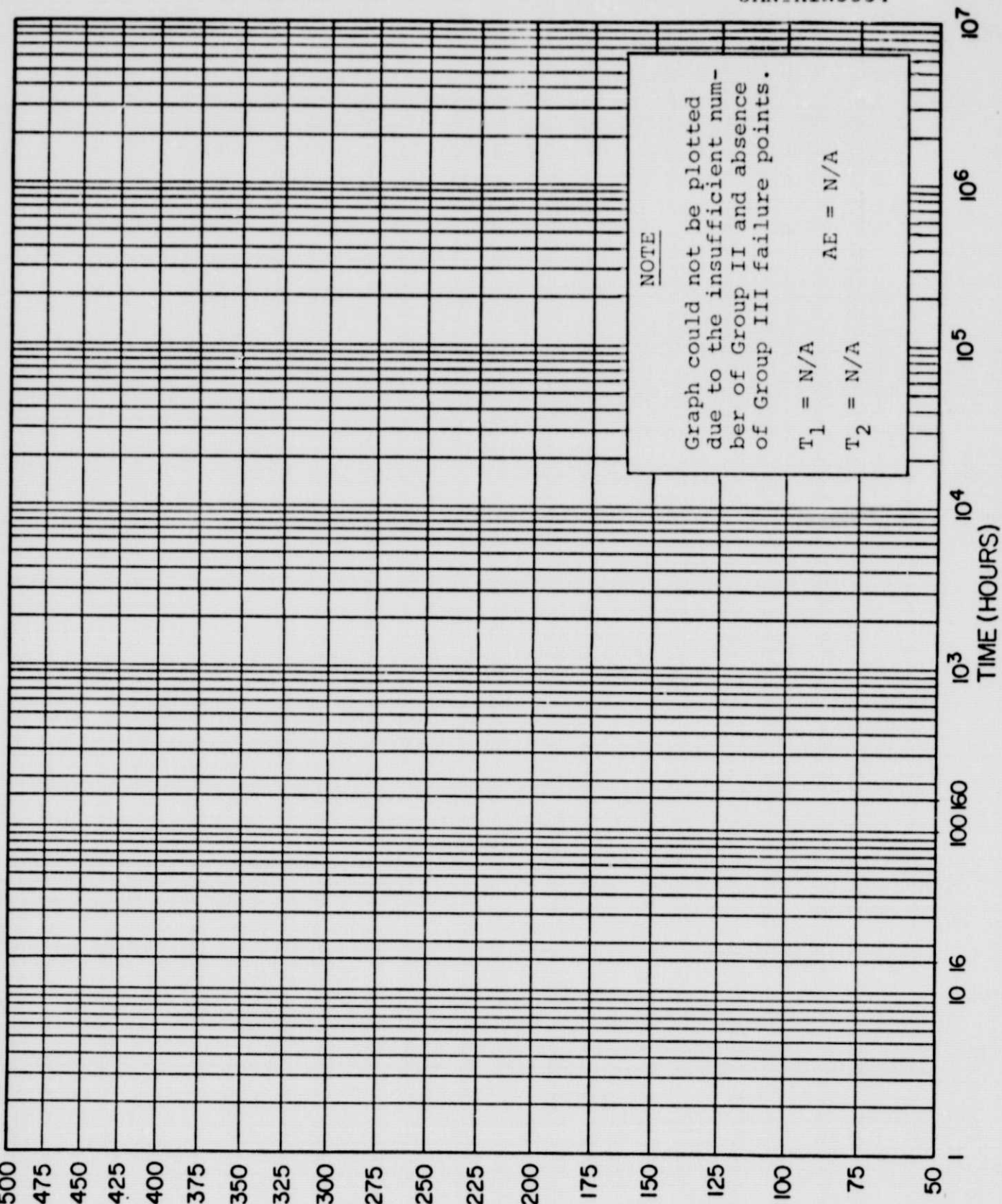
Cumulative Percent Failures Versus Junction Temperature, Micro Semiconductor



\* JUNCTION TEMPERATURE (°C)

\*NOTE

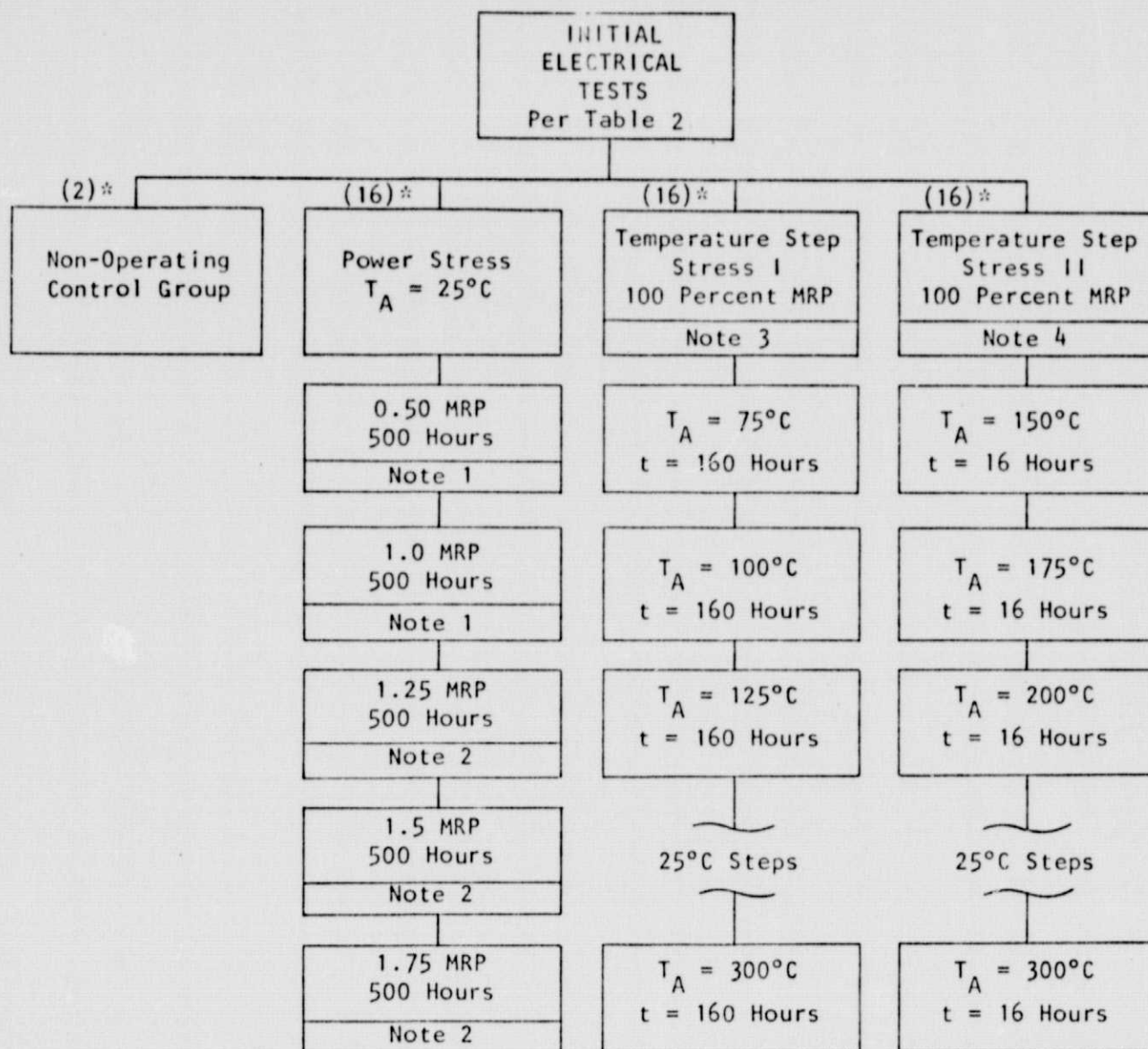
$$T_J \approx T_A + 175^\circ\text{C}$$



Time Steps Versus Junction Temperature, Micro Semiconductor

FIGURE 5



TABLE 1  
TEST FLOW DIAGRAM

\*Quantity per manufacturer (Semtech and Micro Semiconductor)

## NOTES:

- 1) Electrical measurements per Table 2 were made at 50, 150, 250 and 500 hours.
- 2) Electrical measurements per Table 2 were made at 10, 25, 50, 150, 250 and 500 hours.
- 3) Electrical measurements per Table 2 were made at the end of each 160 hours.
- 4) Electrical measurements per Table 2 were made at the end of each 16 hours.





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TABLE 2 Parameter and Test Conditions

PARAMETER	CONDITIONS	SPECIFICATION LIMIT		CATASTROPHIC* LIMIT		UNIT
		MIN	MAX	MIN	MAX	
$I_R$	@ $V_R=1000V$		1.0		100	$\mu A$
$V_{F1}$	@ $I_F=9.0(PK)$ PULSED	.6	1.3	.3	1.95	V(PK)
$V_{F2}$	@ $I_0=2.0A$ NOT PULSED	.6	1.2	.3	1.8	V

\* In addition, any open or short shall be considered catastrophic

TABLE 3 Power Stress Burn-In Conditions

$V_F=1.0V$	
$I_F=$	% $P_D$
1.8A	50
3.6A	100
4.5A	125
5.4A	150
6.3A	175



NOTE  
FOR TABLES  
4 THROUGH 7

The minimum/maximum initial and final data generally have an absolute accuracy of  $\pm 1\%$  of the reading and  $\pm$  one digit except for readings greater than 9.99mA which have an absolute accuracy of  $\pm 2\%$  of the reading and  $\pm$  one digit. The data also has a resolution for four digits. The standard deviations, means, delta means, and average means are, therefore, valid indicators of trends over time and temperature, excepting the minor statistical computer error of supplying a constant number of significant digits.



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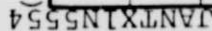
TABLE 4  
GROUP I - POWER STRESS DATA SUMMARY

Page 1 of 2

PARAMETER	$I_R = 1.0 \mu A (MAX)$		$V_{F1} = .6V (MIN) \quad 1.3V (MAX)$		$V_{F2} = .6V (MIN) \quad 1.2V (MAX)$	
CONDITIONS AND LIMIT	@ $V_R = 1000V$		@ $I_F = 9.0A (PK) \quad PULSED$		@ $I_0 = 2.0A \quad (NO^+ \quad PULSED)$	
IDENTIFICATION	SEM	MSC	SEM	MSC	SEM	MSC
INITIAL DATA						
MIN VALUE	56.90nA	29.70nA	.999V	.983V	797.0mV	835.0mV
MAX VALUE	362.00nA	149.00nA	1.180V	1.070V	840.0mV	856.0mV
MEAN	163.50nA	51.90nA	1.106V	1.033V	821.9mV	841.1mV
STD DEV	84.82nA	28.45nA	.052V	.026V	10.02mV	4.8mV
INTERIM DATA						
POWER 50 TO 125% $\Delta$ MEAN VALUE						
50% POWER						
50 Hours	-1.5nA	+9.49nA	+0.017V	+0.012V	+0.5mV	+0.5mV
150 Hours	-3.9nA	+16.19nA	+0.015V	+0.013V	+1.2mV	-.5mV
250 Hours	-1.6nA	+21.41nA	+0.024V	+0.016V	+0.3mV	-.6mV
500 Hours	-8.5nA	+17.99nA	+0.025V	+0.019V	+1.2mV	+1.2mV
100% POWER						
550 Hours	+88.9nA	+9.17nA	+0.023V	+0.013V	-1.8mV	-1.2mV
650 Hours	+134.7nA	+22.50nA	+0.025V	+0.018V	+0.6mV	+0.2mV
750 Hours	+171.5nA	+15.34nA	+0.028V	+0.025V	+3.7mV	+3.0mV
1000 Hours	+3.14mA	+13.69nA	+0.015V	-.005V	-14.1mV	-17.3mV
125% POWER						
1010 Hours	+179.5nA	+10.22nA	+0.028V	+0.019V	+1.8mV	+1.5mV
1025 Hours	+215.2nA	+9.93nA	+0.034V	+0.026V	+6.5mV	+4.5mV
1050 Hours	+604.3nA	+13.38nA	+0.030V	+0.026V	+3.0mV	+2.2mV
1150 Hours	+2.93mA	+14.94nA	+0.017V	-.002V	-12.6mV	-11.5mV
1250 Hours	+2.13mA	-2.09nA	+0.035V	-.029V	+10.4mV	+5.8mV
1500 Hours	+158.94 $\mu A$	+24.26nA	-.067V	-.071V	-118.8mV	+6.3mV

(continued on second sheet)

JANTX1N5554



NOTE: Catastrophic Rejects removed from data.



TABLE 5

JANTX1N5554

**NOTE: CATASTROPHIC REJECTS REMOVED FROM DATA**

TABLE 6

## GROUP III TEMP STRESS II DATA SUMMARY

PARAMETERS	$I_R = 1.0 \mu A (MAX)$	$V_{F1} = .6V (MIN)$	$1.3V (MAX)$	$V_{F2} = .6V (MIN)$	$1.2V (MAX)$
CONDITIONS AND LIMITS	$@V_R = 1000V$	$@I_F = 9.0A (PK)$	PULSED	$@I_0 = 2.0A$	(NOT PULSED)
IDENTIFICATION	SEM	MSC	SEM	MSC	MSC
INITIAL DATA					
MIN VALUE	66.6nA	27.50nA	1.060V	860.0mV	876.0mV
MAX VALUE	742.0nA	484.00nA	1.240V	912.0mV	922.0mV
MEAN	202.0nA	73.13nA	1.119V	881.6mV	886.0mV
STD DEV	175.8nA	106.80nA	.049V	13.0mV	10.6mV
INTERIM DATA (INITIAL TO FINAL)					
$\Delta$ MEAN VALUE					
Total Hrs. Temp.					
16 150°C	+6.65 $\mu A$	-1.17nA	+0.022V	+9.7mV	+8mV
32 175°C	+5.86 $\mu A$	-14.72nA	+0.025V	+12.8mV	+2.9mV
48 200°C	+15.41 $\mu A$	-15.48nA	+0.030V	+16.3mV	+1.5mV
64 225°C	Job Stopped	-25.90nA	Job Stopped	Job Stopped	+3.3mV
80 250°C		-15.39nA			+1.7mV
96 275°C		+1.19 $\mu A$			+4.0mV
112 300°C		+4.68 $\mu A$			+1.8mV
FINAL DATA					
FINAL TEMP	200°C	300°C	200°C	200°C	300°C
MIN VALUE	91.00nA	29.60nA	1.080V	864.00mV	879.00mV
MAX VALUE	134.00 $\mu A$	34.60 $\mu A$	1.380V	1.04V	914.00mV
MEAN	15.61 $\mu A$	4.75 $\mu A$	1.149V	897.90mV	887.80mV
STD DEV	36.47 $\mu A$	9.06 $\mu A$	.078V	40.88mV	9.05mV

NOTE: CATASTROPHIC REJECTS REMOVED FROM DATA

JANTX1N5554



FINAL DATA SUMMARY  
TABLE 7

PARAMETER	SPECIFICATIONS LIMIT		U N I T S	MEAN INT. DATA	AVERAGE			IN MEAN VALUE		
					SEM	MSC	SEM	MSC	SEM	MSC
	MIN	MAX			POWER STRESS		TEMP STRESS I		TEMP STRESS II	
I <sub>R</sub>		1.0	μA		-462.09	-29.779	-173.58	-13.968	-6.9295	-.71553
V <sub>F1</sub>	.6	1.3	V		+.04090	+.02838	+.09940	+.08664	+.26050	+.12338
V <sub>F2</sub>	.6	1.2	V		+.05037	+.03103	+.09231	+.07952	+.21070	+.10875

JANTX1N5554

\* CATASTROPHIC REJECT(S) REMOVED FROM DATA





TABLE 8 STEP STRESS

CATASTROPHIC

FAILURE SUMMARY

JAN TX1N5554

## GROUP I POWER STRESS

TEST STEP	MFR A		MFR B	
	QTY.	NOTE	QTY.	NOTE
50% 50 hr.	0	-	0	-
100 hr.	0	-	0	-
100 hr.	0	-	0	-
250 hr.	0	-	0	-
100% 50 hr.	0	-	0	-
100 hr.	0	-	0	-
100 hr.	0	-	0	-
250 hr.	1	A	0	-
125% 10 hr.	0	-	0	-
15 hr.	0	-	0	-
25 hr.	0	-	0	-
100 hr.	0	-	0	-
100 hr.	0	-	0	-
250 hr.	1	A	0	-
150% 10 hr.	0	-	0	-
15 hr.	0	-	0	-
25 hr.	0	-	0	-
100 hr.	1	A	0	-
100 hr.	1	B	0	-
250 hr.	0	-	0	-
175% 10 hr.	0	-	2	B
15 hr.	0	-	1	A
25 hr.	0	-	0	-
100 hr.	0	-	3	B
100 hr.	0	-	1	A
250 hr.	0	-	Job Stopped	

## GROUP II 160 HR. TEMP. STEPS

TEST STEP T	MFR A		MFR B	
	QTY.	NOTE	QTY.	NOTE
75°C	0	-	0	-
100°C	0	-	0	-
125°C	0	-	0	-
150°C	0	-	0	-
175°C	1	A	0	-
200°C	4	A	0	-
225°C	0	-	0	-
250°C	0	-	0	-
275°C	4	A	0	-
300°C	Job Stopped		2	A

NOTES:

(A)  $I_R > 100 \mu A$ 

\* (B) VISUAL

(C) NOTE (A)  $V_{F1} \& V_{F2} < .3V$ 

## GROUP III 16 HR. TEMP. STEPS

TEST STEP T	MFR A		MFR B	
	QTY.	NOTE	QTY.	NOTE
150°C	0	-	0	-
175°C	0	-	0	-
200°C	1	A	0	-
225°C	Job Stopped		0	-
250°C			0	-
275°C			0	-
300°C			0	-

MFR. "A" = SEMTECH

MFR. "B" = MICRO SEMICONDUCTOR

JANTX1N5554

\*ANODE LEAD DETACHED FROM THE STRESS.





JAN TX1N5554

JANTX1N5554

## FAILURE SUMMARY

PARAMETRIC

STEP STRESS 9

## GROUP I POWER STRESS

TEST STEP	MFR A		MFR B	
	QTY.	NOTE	QTY.	NOTE
50% 50 hr.	0	-	0	-
100 hr.	0	-	0	-
100 hr.	0	-	0	-
250 hr.	0	-	0	-
100% 50 hr.	1	A	0	-
100 hr.	0	-	0	-
100 hr.	0	-	0	-
250 hr.	0	-	0	-
125% 10 hr.	1	A	0	-
15 hr.	0	-	0	-
25 hr.	1	A	0	-
100 hr.	0	-	0	-
100 hr.	1	A	0	-
250 hr.	0	-	0	-
150% 10 hr.	0	-	0	-
15 hr.	1	B	0	-
25 hr.	1	C	0	-
100 hr.	1	A	0	-
100 hr.	0	-	1	A
250 hr.	3	A	0	-
175% 10 hr.	0	-	0	-
15 hr.	0	-	2	A
25 hr.	0	-	0	-
100 hr.	0	-	5	A
100 hr.	2	A	1	A
250 hr.	0	-	Job Stopped	

## GROUP II 160 HR. TEMP. STEPS

TEST STEP	MFR A		MFR B	
	QTY.	NOTE	QTY.	NOTE
75°C	1	A	0	-
150°C	0	-	0	-
125°C	0	-	0	-
150°C	0	-	0	-
175°C	1	A	0	-
200°C	2	A	0	-
225°C	0	-	0	-
250°C	0	-	0	-
275°C	0	-	14	A
300°C	Job Stopped		1	A

## GROUP III 16 HR. TEMP. STEPS

TEST STEP	MFR A		MFR B	
	QTY.	NOTE	QTY.	NOTE
150°C	4	A	0	-
175°C	0	-	0	-
200°C	4	A	0	-
225°C	Job Stopped		0	-
250°C			0	-
275°C			4	A
300°C			2	A

MFR. "A" = SEMTECH

MFR. "B" = MICRO SEMI CONDUCTOR

## NOTES:

- (A)  $I_R$  MAXIMUM LIMIT FAILURE  
(B)  $V_{FI}$  MAXIMUM LIMIT FAILURE  
(C) S/N 6827 VISUAL DUE TO HANDLING  
(D) NOTES (A) and (B)  
(E) S/N 6821 MISSING FROM SAMPLE LOT



APPENDIX A

Failure Analysis

Power Stress



MFSC STEP-STRESS TEST  
FAILURE ANALYSIS  
DIODES

JANTX1N5554

Date 2 November 1978

J/N 2CN242-23A P/N 1N5554

MFR Micro Semiconductor

Limit: 1.0uA Max.

Limits: 0.6 - 1.2 V

FAILURE VERIFICATION:

S/N	PIV -volts-	$I_r$ @ 1000V.dc	$V_f$ @ 2.0 A dc				Initial Rej. @ Test Seq. No.:	Initial Rej. for
6853	210 (R)	$\infty$	0.60				MP-23	$I_R$
6856	1100	2 uA	0.73				MP-25	$I_R$
6859	1100	0.5 uA	0.65				MP-22	Lead Off

VISUAL INSPECTION.

All three Micro Semiconductor samples have lost their external paint and have a burnt area on one lead where it was held in the burn-in clip.

S/N 6853 has cracked glass (see Figure A-1).

S/N 6856 has lost its external anode lead (see Figure A-2).

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\*h<sub>FE</sub> trace present. Cannot meet stated test conditions. (Leaky)  
\*h<sub>FE</sub> trace very leaky.

= drift H = hysteresis Inv = inversion R = resistive S = soft Uns = unstable



MFSC STEP-STRESS TEST  
FAILURE ANALYSIS

JANTX1N5554

DIODES

Date 2 November 1978

J/N 2CN242-23A P/N 1N5554 MFR Semtech

Limit: Limits:  
FAILURE VERIFICATION: 1.0uA Max. 0.6 - 1.2 V

S/N	PIV -volts-	$I_r$ @ 1000V.dc	$V_f$ @ 2.0 A dc				Initial Rej. @ Test Seq. No.:	Initial Rej. for
5824	1100	1.0uA	0.70				MP-19	$I_R$
6902	940		0.65				MP-20	$I_R$
6906	900		0.62				MP-20	$I_R$

VISUAL INSPECTION.

All three Semtech samples have lost their external paint and have a burnt area on one lead where it was held in the burn-in clip (see Figure A-3).

S/N 6824 has lost its external anode lead (see Figure A-4).

\* $h_{FE}$  trace present. Cannot meet stated test conditions. (Leaky)  
\* $h_{FE}$  trace very leaky.

D = drift H = hysteresis Inv = inversion R = resistive S = soft Uns = unstable





JANTX1N5554

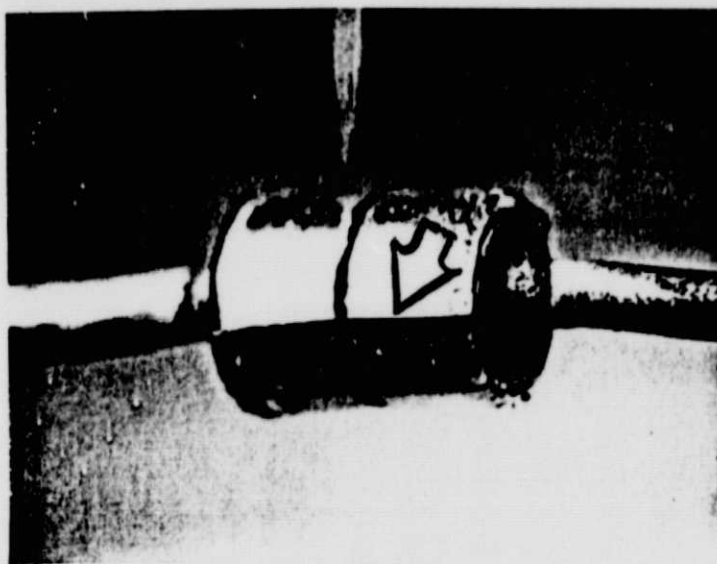


FIGURE A-1  
S/N 6853 Micro Semiconductor  
Sample Showing Cracked Glass, 8X

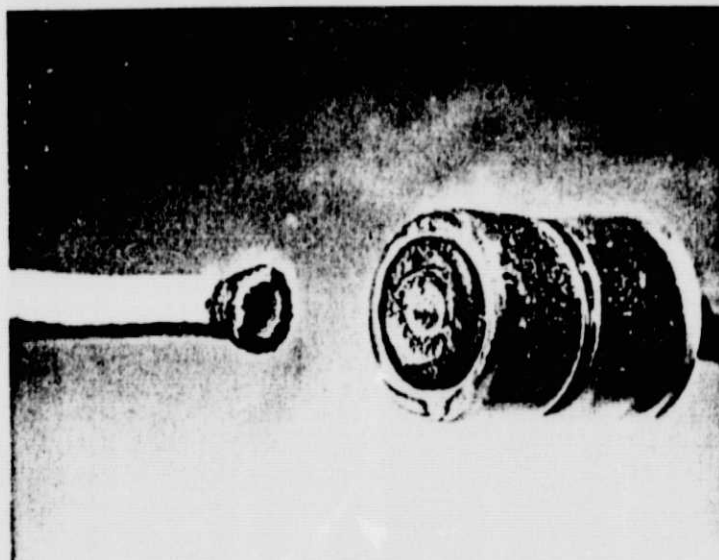


FIGURE A-2  
S/N 6856 Micro Semiconductor  
Sample Showing Lost Anode Lead, 8X  
(Similar to S/N 6859)

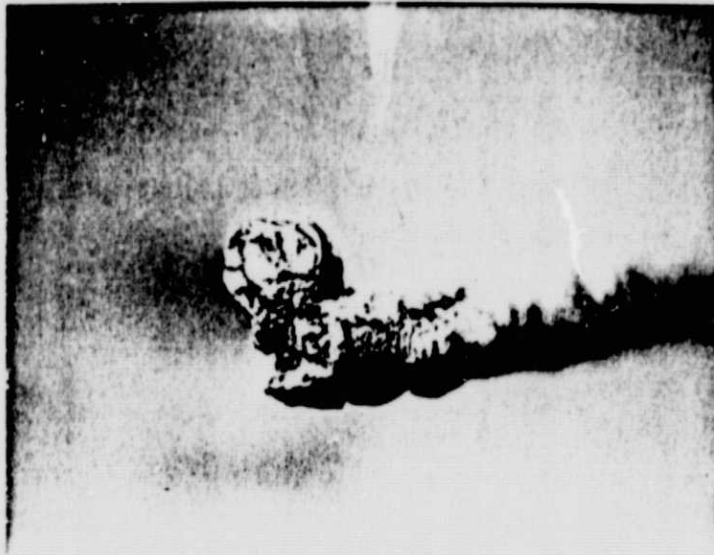


FIGURE A-3  
S/N 6824 Semtech Sample  
Showing Anode Lead Melted at the Point of  
Contact to the Burn-in Clip, 11X

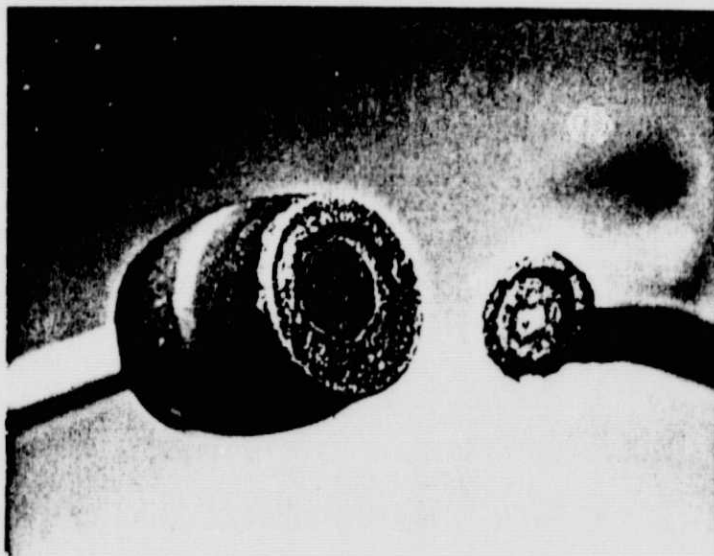


FIGURE A-4  
S/N 6824 Semtech Sample  
Showing Lost Anode Lead, 8X



## CONCLUSIONS

### Micro Semiconductor

S/N 6856 and 6859 were still within the electrical limits of the MSFC test when they became visual failures due to loss of their anode leads. This suggests that these structural failures were caused by exceeding the thermal design limits of the parts.

S/N 6853 has a damaged junction due to electrical over-stress, and cracked glass.

### Semtech

S/N 6824 was electrically acceptable to the MSFC test limits when its lead detached due to exceeding the melting point of the lead connecting metal.

S/N 6902 and 6906 failed for excess reverse leakage current because the peak inverse voltage (PIV) of both samples is less than the 1000-volt test condition. (See electrical data in Failure Verification section above.)

The hard, stable breakdown of these samples indicates that there is no junction damage. The most probable cause of the lowered breakdown voltage on these samples is a change in the concentration of surface impurities on the P-N junction.

When there is a slight concentration of impurities of the same polarity as the high resistivity side of the junction (not sufficient to cause inversion) then that resistivity will be raised. This will in turn raise the breakdown voltage. Upon migration of these protective charges away from the vicinity of the junction, the resistivity and the breakdown will fall.



JANTX1N5554

The hard breakdown curves of these two samples, taken together with their acceptable leakage levels at 1000 volts bias during earlier test sequences, suggests that the surface charge migration mechanism, as described above, was the cause of the failures.





APPENDIX B

Failure Analysis

Temperature Stress



MSFC STEP-STRESS TEST  
FAILURE ANALYSIS

JANTX1N5554

DIODES

Date 3 November 1978

J/N 2CN242-23B P/N 1N5554 MFR Semtech

FAILURE VERIFICATION: Limit: 1.0 uA Max. Limits: 0.6-1.2 V

S/N	PIV -volts	$I_r$ @ 1000 V.dc	$V_f$ @ 2.0 A dc	Initial Rej. @ Test Seq. No.:	Initial Rej. for
6834	600 1100 (S)	400 uA	0.69 V	MP-2	$I_R$ , $V_f$
6914	1040 930 (Uns)	$\infty$	0.69	MP-7	$I_R$
916	940	$\infty$	0.66	MP-2	$I_R$

VISUAL INSPECTION.

All the samples have lost their external paint. There are no other significant defects (see Figure B-1).

CONCLUSIONS.

The action of the curve trace while measuring PIV on these parts indicates a condition of surface instability due to contamination which can move under the influence of temperature and bias.

These samples are  $I_R$  rejects when measured at 1000 volts because their breakdowns have drifted below 1000 volts. The surface action which resulted in this voltage drift is the same as that described in Appendix A.

\*h<sub>FE</sub> trace present. Cannot meet stated test conditions. (leaky)  
\*\*h<sub>FE</sub> trace very leaky.

D = drift H = hysteresis Inv = inversion R = resistive S = soft Uns = unstable



JANTX1N5554

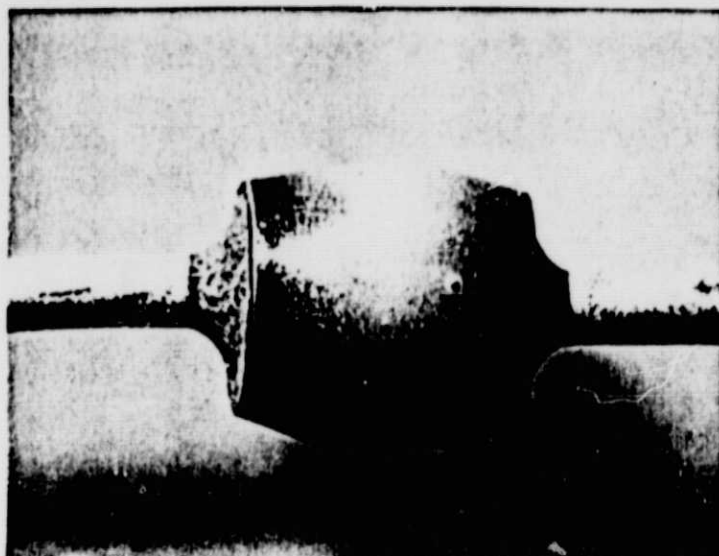


FIGURE B-1  
S/N 6916 Typical Semtech Diode, 10X

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